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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,886	08/26/2003	Monte Manning	MI22-2374	4873

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WELLS ST. JOHN P.S.
601 W. FIRST AVENUE, SUITE 1300
SPOKANE, WA 99201

EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,886	MANNING, MONTE	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *40-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *40-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/R strictions

Applicant's election without traverse of claims 40-58 on 5/20/2004 is acknowledged.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 40-58 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-24 of U.S. Patent No. 6,611,059. Although the conflicting claims are not identical, they are not patentably distinct from each other. Claims 40-58 are broader than corresponding claims 1-24 of U.S. Patent No. 6,611,059, and thus allow unjustified or improper timewise extension of the "right to exclude" granted by U.S. Patent No. 6,611,059.

Claim R j ctions - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 40-58 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of a series of alternating first and second conductive lines, wherein first lines and second lines having respective line tops, as recited in claims 40 and 48, and a series of first conductive polysilicon lines, first series conductive lines, and the lines, as recited in claim 56, are unclear as to whether the first mentioned conductive lines are the second mentioned lines.

The claimed limitation of a respective insulating oxide material, as recited in claim 56, is unclear as to whether the respective insulating oxide material is the insulative oxide material, or it is a separate layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 40-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al. (5,413,962) in view of Choe (5,583,357).

Lur et al. teach in figure 11 and related text an Integrated circuitry comprising: a semiconductive substrate 20; an electrically insulating layer 22, 23 over the semiconductive substrate; and a series of alternating first and second conductive lines 24 spaced and positioned laterally adjacent one another over the insulating layer, the first lines and the second lines having respective line tops, and being electrically isolated from one another laterally by intervening insulating spacers having respective spacer tops that are substantially coplanar with at least some of the first and second line tops.

Lur et al. do not explicitly state that the spacers are insulating spacers.

Choe teaches in figure 11A and related text insulating spacers 5. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use insulating spacers in Lur et al.'s device in order to provide protection for the device.

Regarding claims 41 and 49, Lur et al. teach in figure 11 and related text at least some of the individual laterally adjacent first and second series lines are disposed directly on the electrically insulating layer.

Regarding claims 42 and 50, Lur et al. teach in figure 11 and related text the first lines have a substantially common lateral cross sectional shape and the second lines have a substantially common lateral cross sectional shape, wherein Choe teaches in figure 11A and related text first lines' lateral cross sectional shape being different from the second lines' lateral cross sectional shape. It would have been obvious to a person of ordinary

skill in the art at the time the invention was made to use first lines' lateral cross sectional shape being different from the second lines' lateral cross sectional shape in Lur et al.'s device in order to simplify the processing steps of making the device by forming the lines at constant intervals.

Regarding claims 43 and 51, Lur et al. teach in figure 11 and related text the first and second conductive lines constitute the same materials.

Regarding claims 44, 46, 52 and 54, Lur et al. teach in figure 11 and related text the first 24 and second 40 conductive lines constitute different materials, wherein the first conductive lines predominately comprise doped polysilicon and the second conductive lines predominately comprise metal.

Regarding claims 45 and 53, Lur et al. do teach in figure 11 first conductive lines predominately comprise undoped polysilicon. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use first conductive lines predominately comprise undoped polysilicon in Lur et al.'s device in order to adjust the conductivity of the lines according to the application at hand.

Regarding claims 47 and 55, Lur et al. teach in figure 11 and related text a plurality of the series of the first and second conductive lines at multiple elevations relative to the substrate.

Regarding claim 48, Lur et al. teach in figure 11 and related text first and second lines having respective lateral widths and being spaced and positioned laterally adjacent one another, the first lines and the second lines being electrically isolated and separated from one another laterally by intervening strips of spacer material having respective individual material lateral widths that are substantially less than the lateral widths of any of the first and second conductive lines, and none of the first and second lines overlapping any immediately laterally adjacent first or second lines.

Claims 56-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chu (5,519,239) in view of Miyanaga et al. (5,418,187).

Regarding claim 56, Chu teaches in figure 3O and related text an Integrated circuitry comprising: a semiconductive substrate 300; a series of first conductive polysilicon lines 302 (see figure 3H) over the substrate, the first series conductive lines having individual pairs of respective sidewalls; electrically insulative oxide material 304 over respective first series conductive lines, a top of the oxide material over at least some of the lines defining a first plane; a plurality of insulative oxide sidewall spacer pairs 311, individual spacer pairs being on respective sidewall pairs of individual first series conductive lines and being connected with the electrically insulating oxide material over the respective individual first series conductive lines; individual first series conductive lines being

effectively insulated by the gate oxide layer 301, the respective sidewall spacer pairs 311, and the respective insulating oxide material; and

a series of second conductive aluminum-containing lines 303 having respective line tops at least some of which define a second plane that is coplanar with said first plane, the series of second conductive lines being over the substrate.

Chu does not teach an electrically insulative borophosphosilicate glass (BPSG) layer over the semiconductive substrate. Miyanaga et al. teach in figure 1E an electrically insulative borophosphosilicate glass (BPSG) layer 11 over the semiconductive substrate 100. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an electrically insulative borophosphosilicate glass (BPSG) layer over the semiconductive substrate of Chu's device in order to promote surface tension and to obtain higher yield and reliability. The combination is motivated by the teachings of Miyanaga et al. who point out the advantages of using an electrically insulative borophosphosilicate glass (BPSG) layer over the semiconductive substrate (column 2, lines 13-68, and column 9, lines 5-12).

Regarding claim 57, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use first series conductive lines having elevational thicknesses in a range from 2000 Angstroms to 10,000 Angstroms in Chu's device, since it is within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claim 58, Chu teaches in figure 3O and related text individual second series lines have substantially a common lateral cross sectional shape.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
6/1/04

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800